Multi-channel Timing Interval Measurement System Based on FPGA

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Abstract: In this paper, the synchronous time interval measurement system of multichannel timing generator based on FPGA is introduced. FPGA is used to measure the time interval of 42 high-precision timing signals, and TCP/IP interface is used to display between the machine and computer. Hardware design of time interval measurement system and the selection of measurement mode of upper computer are emphasized. The design can ensure that the timing measurement error of each channel is less than 1us, which has multiple timing measurement methods. The system has the advantages of high precision, simple operation and good applicability, which has been successfully applied to the front line of timing measurement in military shooting range.

1. Introduction

With the development of modern weapons and equipment towards the direction of long-range strike, precise guidance, digitalization and unmanned, the modern military range is required to have more advanced testing technology. As an indispensable part of testing the performance of modern weapons and equipment, timing interval measurement system technology has been widely used in modern military weapons and equipment, social life and other fields. [1] However, most modern timing interval measurement systems are single control of measurement or test control by computer. Such systems have single function, complex structure and high cost, which are not suitable for modern military shooting range environment. At the same time, the artificial and inefficient timing interval measurement method for short range and unguided weapons can no longer meet the requirements of accurate test and measurement of new equipment.

The timing interval measurement system makes full use of FPGA's high-speed programmable logic processing capacity. The FPGA-based hardware platform achieves 42-channel high-precision timing interval measurement. This system has simple circuits, low power consumption, flexible measurement methods, good compatibility, scalability, and portability, which can accurately measure time intervals of multiple channels. Details on hardware design and software design are discussed in later sections.

2. Working principle of system

This system is consisted of four parts: input interface and reference signal generating part, communication part, host computer display part and mode selection part. The timing signals of 42 channels are received through the input interface. The measured signals are performed through hardware filtering to improve the signal accuracy. The time interval between each level change on any channel and the reference signal are calculated. Upload the measured time interval of each channel to the host computer for display through TCP/IP communication. At the same time, the host

computer selects the measured signal mode and supports the measurement of level and on-off signals. The system works as shown in Figure 1.

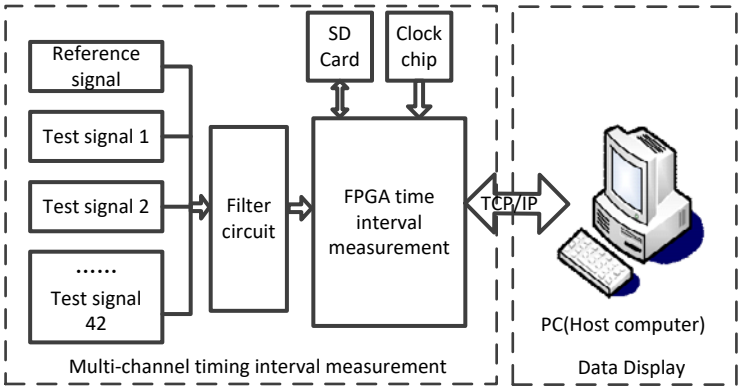

Figure 1. Working principle of system

3. Hardware design

Multi-channel timing interval measurement hardware consists of CPU master control module, power module, input interface module, benchmark signal generation module, data storage module, clock module, TCP/IP communication module, etc.

This system takes FPGA as the main control platform, and EP2C5T144C8 chip of Cyclone series of Altera company is selected. According to the actual measurement requirements of the system and the actual module building test, three voltages of +5V, + 3.3V and + 1.5V are needed to supply the voltage of the system, which is power module. The external supply voltage is converted to the voltage value required by the system through the LM317 converter chip. For the 42-channel timing signal input interface module, the system uses a 6N137 chip to perform hardware filtering on the timing signals to improve the stability and accuracy of the signals to be processed. In order to ensure the accuracy of the signal, subsequent signals are connected to the 6N137 chip to perform hardware filtering on the reference signal. The time information provided by PCF8563 is stored in the SD card as a timestamp to facilitate later data analysis. The hardware block diagram is shown in Figure 2.

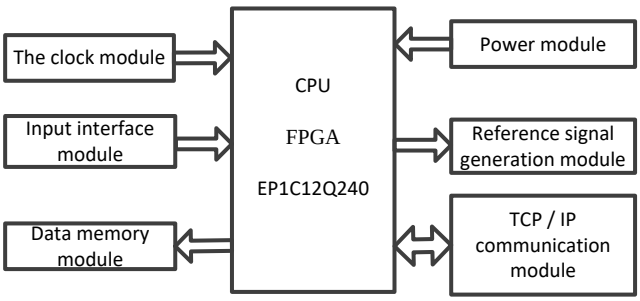

Figure 2. Hardware design of block diagram

4. Software Design

4.1 Controller software

The controller software is written in the QuartusII5.1 integrated development environment, and the hardware description language VerilogHDL is used for on-line programming. The main control unit program includes the reference signal generation subroutine, the channel signal detection subroutine, the data storage subroutine, TCP/IP communication subroutine and so on. After the system is powered on, it performs a self-test. The host computer software writes the configured 40-channel parameters to the controller through TCP/IP communication interface. The main control program software flowchart is shown in Figure 3.

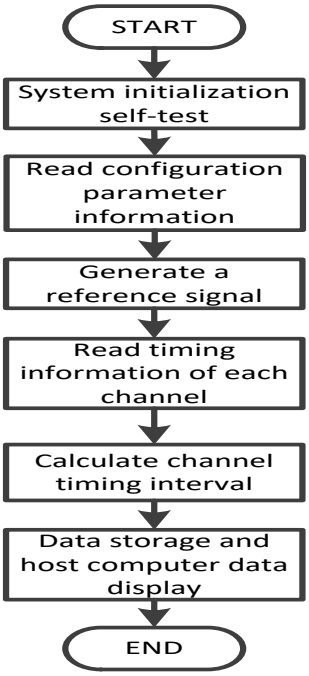

Figure 3. Flow chart of master control software

4.2 PC Software Design

The PC software on the system is implemented on the Visual Studio 2012 development platform using the C# programming language. It has the function of timing measurement parameter configuration, selection of the type of measured signal, real-time display of the measured time and excel table storage.

The host computer uses the TCP/IP protocol to establish a connection with the timing measurement system. The host computer which has a fixed IP address and a communication port acts as a server in communication. There are 20 channels, with four kinds of timing signal “on / off / off / level trigger”, which can be measured by controller and sent to PC software. Also, the measured time interval of each channel will be displayed on each blank place. The software interface of the host computer is shown in Figure 4.

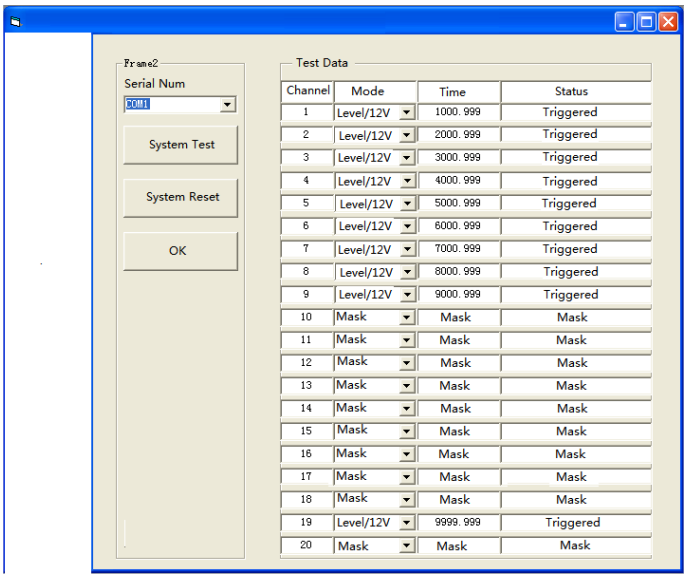

Figure 4. Interface diagram of host computer software

5. Conclusion

This paper provide a synchronous time interval measurement system based on an FPGA-based multi-channel timing generator. The system fully benefits the FPGA's high-speed programmable logic processing capabilities and improves system flexibility and stability. This design can ensure that the timing signals of 20 channels are measured by the external trigger signal as the reference time interval measurement. After a large number of repeated experiments, the test results show that the measurement timing error of each channel of the system is less than 1 us. This method has been successfully applied in military shooting range test systems. The design has very good use value in stability and real-time performance, so the promotion of this system has important practical significance.

Acknowledgements

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